

Search Results

Results for "((i/o and evaluation and cell)<in>metadata)"

Your search matched 4 of 1430374 documents.

A maximum of 100 results are displayed, 25 to a page, sorted by Relevance in Descending order.

[e-mail](#) [Printer friendly](#)

» Search Options

[View Session History](#)[New Search](#)

Modify Search

((i/o and evaluation and cell)<in>metadata)

[Search](#)

» Key

IEEE JNL IEEE Journal or Magazine

IEE JNL IEE Journal or Magazine

IEEE CNF IEEE Conference Proceeding

IEE CNF IEE Conference Proceeding

IEEE STD IEEE Standard

[View selected items](#) [Select All](#) [Deselect All](#)

- 1. **25 ps/gate GaAs standard cell LSIs using 0.5 μm gate MESFETs**
Nemoto, M.; Ogawa, Y.; Morita, Y.; Seki, S.; Kawakami, Y.; Akiyama, M.;
Gallium Arsenide Integrated Circuit (GaAs IC) Symposium, 1992. Technical Digest 1992.. 14th Annual IEEE
4-7 Oct. 1992 Page(s):93 - 96
Digital Object Identifier 10.1109/GAAS.1992.247215
[AbstractPlus](#) | Full Text: [PDF\(284 KB\)](#) [IEEE CNF](#)
[Rights and Permissions](#)

- 2. **VLSI implementation of digit-recurrent CORDIC with constant scaling factor**
Shen-Fu Hsiao; Jen-Yin Chen;
Circuits and Systems, 1997. ISCAS '97.. Proceedings of 1997 IEEE International Symposium on
Volume 3, 9-12 June 1997 Page(s):2068 - 2071 vol.3
Digital Object Identifier 10.1109/ISCAS.1997.621563
[AbstractPlus](#) | Full Text: [PDF\(312 KB\)](#) [IEEE CNF](#)
[Rights and Permissions](#)

- 3. **High density radiation hardened FeRAMs on a 130 nm CMOS/FRAM process**
Kamp, D.A.; DeVilbiss, A.D.; Haag, G.R.; Russell, K.E.; Derbenwick, G.F.;
Non-Volatile Memory Technology Symposium, 2005
7-10 Nov. 2005 Page(s):4 pp.
Digital Object Identifier 10.1109/NVMT.2005.1541393
[AbstractPlus](#) | Full Text: [PDF\(234 KB\)](#) [IEEE CNF](#)
[Rights and Permissions](#)

- 4. **ATR's artificial brain ("CAM-Brain") project: A sample of what individual "CoDi-1 Bit" model evolved neural net modules can do with digital and analog I/O**
de Garis, H.; Buller, A.; Korkin, M.; Gers, F.; Nawa, N.E.; Hough, M.;
Evolvable Hardware, 1999. Proceedings of the First NASA/DoD Workshop on
19-21 July 1999 Page(s):102 - 110
Digital Object Identifier 10.1109/EH.1999.785441
[AbstractPlus](#) | Full Text: [PDF\(88 KB\)](#) [IEEE CNF](#)
[Rights and Permissions](#)

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L5	29	i/o near9 cell same (arrangement or arrang\$4) same periphe\$3 same core	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/11/06 12:23
L6	745355	power near9(rout\$4 or connect\$4 or interconnect\$4)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/11/06 12:23
L7	9	L5 and L6 and pad	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/11/06 12:24
L8	0	evaluat\$4 same (cell or layout or area) and l7	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/11/06 12:27
L9	0	determin\$4 same (cell or layout or area) and l7	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/11/06 12:27